THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KENICHI ASANO and RYUTA SUZUKI

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Appeal No. 1996-2197
Application 08/150,548

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ON BRIEF[1]

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Before JERRY SMITH, DIXON and FRAHM, Administrative Patent Judges.

FRAHM, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 5 to 12, which constitute all of the claims pending on appeal. Claims 1 to 4 stand withdrawn as

[1] Oral Hearing was scheduled for the instant appeal in this case for February 9, 2000. After submitting confirmation in writing on January 13, 2000, that appellants' representative would attend appellants' representative failed to attend Oral Hearing. Accordingly, Oral Hearing in this case has been waived, and the case will be decided on brief.

being drawn to non-elected subject matter.

BACKGROUND

The subject matter on appeal is directed to an image processor having plural unit processors which are programmed to be assigned image frame regions. Each of the unit processors has a fetching unit and a processing unit wherein each unit processor is assigned non-contiguous frame regions, and wherein all of the unit processors simultaneously start processing image signals after all of the assigned frame regions have already been fetched (see representative claim 5 on appeal). As indicated by appellants (see specification, page 2; Brief, page 3), it was conventional in the prior art that the frame regions be assigned to the unit processors in a contiguous fashion, and that the processing of input data begin only after all assigned frame regions have been fetched. Appellants recognized that such prior art image processors suffer from the difficulty of not making the best use of the processing capacity of the plural unit processors (see specification, pages 3 to 5). To overcome this problem, appellants provide for non-contiguous assignment of frame

regions, and for simultaneously starting processing of input data after all of the assigned frame regions have been fetched. This overcomes the problem in the prior art of low processing capacity (specification, page 8).

As further discussed, infra, we find that appellants' admitted prior art of Figures 17 to 23, and pages 1 to 8 of the specification corresponding thereto, fails to teach or suggest at least the two salient features of assigning frame regions in a "non-contiguous" manner, and simultaneously starting processing of all of the unit processors after all of the assigned frame regions have been fetched, as defined in representative independent claim 5 on appeal.

Representative independent claim 5 is reproduced below:

5. An image processor having a plurality of unit processors which are programmed to be assigned frame regions of one picture frame, said unit processors each comprising:

a fectching unit for fetching input partial image signals corresponding to the frame regions assigned to the unit processor,

a processing unit for processing the input partial image signals after all of the input partial image signals corresponding to assigned frame regions have been fetched,

means for providing the processed signals to an output bus,

wherein each of said unit processors is assigned a plurality of frame regions which are not contiguous to each other, and

means for causing all the unit processors to simultaneously start processing the input partial image signals after all of the input partial image signals corresponding to the assigned frame regions have been fetched.

Claims 5 to 12 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon appellants' admitted prior art of Figures 17 to 23.

Rather than repeat the positions of appellants and the examiner, reference is made to the Briefs and the Answers for the respective details thereof.

OPINION

It is our view that the prior art relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 5 to 12. We also find that any conclusion of obviousness of the invention as recited in the claims on appeal would necessarily have involved the improper use of hindsight.

In reaching our conclusion on the issues raised in this appeal, we have carefully considered appellants' specification and claims, the applied prior art, and the respective viewpoints of appellants and the examiner. As a consequence of our review, we are in general agreement with appellants (Brief, pages 3 to 6; Reply Brief, pages 1 to 5) that the claims on appeal would not have been obvious to one of ordinary skill in the art at the time the invention was made in light of the teachings of appellants'

Figures 17 to 23. For the reasons which follow, we will not sustain the decision of the examiner rejecting claims 5 to 12 under 35 U.S.C. § 103.

At the outset, we note that it must be recognized that any judgement on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See

In re McLaughlin, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971).

Appellants argue (Brief, pages 3 to 5) that their admitted prior art Figures 17 to 23 fail to teach or suggest assigning non-contiguous frame regions to each unit processor, and instead assigns contiguous regions to each processor. We agree, and we note that the examiner admits that the admitted prior art "does not expressly state the assigned regions are non-contiguous" (Answer, page 3).

As described in their specification, appellants' Figure 17 shows a unit processor (CPU 171) which instructs plural processing units (173a-h) to "transfer data sequentially" (specification, page 2), such that the input data is transfered "for the regions assigned thereto" (specification, page 2). Once the processing units (173a-h) have completed processing for the assigned regions, the unit processor instructs the processing units to start processing "for the subsequent regions" (specification, page 3). In addition, processing of fetched input data must be completed before "subsequent" data can be fetched (see specification, page 6). Thus, the contiguous and sequential nature of conventional

image processors such as that described by appellants in relation to Figures 17 to 23 results in a low processing efficiency of the image processor. Appellants have recognized this difficulty with the prior art, and have increased processing efficiency by assigning non-contiguous frame regions to the unit processors.

We cannot agree with the examiner that the ordinarily skilled artisan "would have adopted such non-contiguous region assignment to achieve less fluctuation in the processing time" (Answer, page 3), especially if it is true that "it makes no difference whether the assigned regions are contiguous or non-contiguous" as the examiner alleges (Answer, pages 3 to 4). The only direction to assign non-contiguous frame regions (instead of contiguous frame regions as previously known) is found in appellants' own disclosure. We find that to modify appellants' admitted prior art image processor of Figures 17 to 23 in order to achieve appellant's claimed invention would have required the use of impermissible hindsight.

We also agree with appellants that "nothing in the admitted prior art suggests starting the processors simultaneously in processing a frame" (Reply Brief, page 4).

We are not persuaded by the examiner's averment that simultaneously starting the processing after all fetching is done is an "inherent feature in the system" (Answer, page 3). We cannot agree with the examiner's circular reasoning (Answer, page 5) that if all sub-regions were merged into one region, then all processing would start simultaneously after all the sub-regions were fetched. The fact is that appellants' admitted prior art, as well as the subject matter on appeal, concern one frame which is made up of plural assigned frame regions or sub-regions. We agree with appellants that "no variations of the prior art system [which does not simultaneously start] are discussed in the specification" and that the "specification does not teach or suggest any variations or modifications" (Reply Brief, page 3). "Nothing in the specification suggests that sub-regions can be eliminated in the prior art systems" (Reply Brief, pages 3 to 4). Accordingly, we find that it would not have been obvious to the ordinary skilled artisan to simultaneously start processing after fetching all of the assigned frame regions as required by representative claim 5 on appeal.

Lastly, we do not agree with the examiner that "any

variation in the processing start time for sub-regions in each frame is an arbitrary design choice" (Answer, page 5), nor do we agree with the examiner that "to simultaneously start the processing after the completion of fetching of data for all regions is a design choice, where the simultaneous starting offers no advantage in processing speed" (Supplemental Answer, page 2). To the contrary, we find that the most significant aspect of appellants' invention recited in the claims on appeal is that it increases processing speed. Appellants specifically point out that the purpose of their invention is to make "the best use of the processing capacity of the parallel arrangement of multiprocessors" so that the processors operate together to "minimize delays due to longer processing times for some portions of the frame" (specification, page 8).

In light of the foregoing, the differences between the subject matter recited in the claims and the applied prior art

are such that the claimed subject matter as a whole would not have been obvious within the meaning of 35 U.S.C. § 103. Accordingly, we shall reverse the standing rejection of claims 5 to 12 on appeal.

REVERSED

JERRY SMITH Administrative Patent Judge	)
JOSEPH L. DIXON Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
ERIC FRAHM Administrative Patent Judge	)

EF/pgg
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